REMARKS

The following remarks are prepared in response to the Office Action mailed January 9, 2003. The Office Action rejected claims 1-11 and 49 under 35 U.S.C. §§ 112 and 102(b). Claims 1-11, 49 and 50 remain pending in the application. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Objection to the Specification

The Office Action objected to the specification as failing to provide proper antecedent basis for the claimed subject matter. In particular, the Office Action recited that the specification fails to include language such as "the position of which does not correspond to a byte boundary" and "cycling through m different values, with m is not being a power of two", as recited in the claims. Applicants herein provide amendments to claims 1 and 49 to remove the objected to language. Therefore, Applicants respectfully request the Examiner to withdraw the objection to the specification in view of the amendments to claims 1 and 49.

Rejections Under 35 U.S.C. § 112, First and Second Paragraphs

The Office Action rejected claims 1-11 and 49 under 35 U.S.C. § 112, first and second paragraphs. Applicants herein provide amendments to claims 1 and 49 to remove the rejected limitations. Accordingly, Applicants respectfully request the Examiner to withdraw the rejections under 35 U.S.C. § 112, first and second paragraphs, to the claims in view of the amendments to claims 1 and 49.

Rejections Under 35 U.S.C. §§ 102(b) and 103(a)

The Office Action rejected claims 1-11 and 49 under 35 U.S.C. § 102(b) as being anticipated by Christie et al. (hereinafter "Christie") (U.S. Patent No. 5,559,975) and claim 49

under 35 U.S.C. § 103(a) as being unpatentable over Christie. Applicants have amended claims 1 and 49 to distinguish over the Christie reference and to more particularly define the invention.

Independent claims 1 and 49 have been amended to recite, in part, a processor for reading instructions from a memory, the memory storing at least one processing packet being made of an integer number of bytes, the processing packet including processing target instructions, the number of processing target instructions being any number except for a power of 2. Support for the amendments to claims 1 and 49 can be found throughout the specification, for example, at page 45, lines 2-16. In addition, independent claims 1 and 49 have been amended to recite, in part, a second program counter indicating a position of processing target instruction in the processing packet by using the same number of values as the number of processing target instructions, and cycling through the values. Hence, the second program counter cycles through the same number of values as the number of processing target instructions which can be any number except for a power of 2. Therefore, when switching occurs from a current processing target instruction to another processing target instruction in a different (or the same) processing packet, the position of the next processing target can be easily and reliably determined by cyclically shifting the values for the number of processing target instructions residing between the current processing target instruction and the next processing target instruction.

On the other hand, the Christie reference discloses, as the second counter, four bits out of a 32-bit counter value. The second counter provides a potential next decode program counter value corresponding to an ROP (RISC operation) from a queue. The second counter includes four bit adders that add a value of four bits from the queue to a value that is based on the byte length of the X86 instruction, and provides the resulting values to the program counter value

selection circuit. (See col. 18, lines 4-23). In addition, the Christie reference discloses an instruction decoder 108 that maintains a decode program counter value for the ROP or ROPs corresponding to each of the X86 instructions in the queue by counting the number of bytes between instruction boundaries. (See col. 16, lines 7-10). Hence, the counter value for each instruction is determined by counting the number of bytes between instruction boundaries.

The Christie reference, however, does not disclose, teach or suggest a second program counter indicating a position of processing target instruction in the processing packet by using the same number of values as the number of processing target instructions, and cycling through the values as recited in independent claims 1 and 49. Therefore, it follows that the Christie reference does not disclose, teach or suggest how to provide a program counter when the number of processing target instructions in a processing packet is a number other than a power of 2. Furthermore, the Christie reference fails to reliably specify a position of a next processing target instruction. For example, when shifting occurs from a processing target instruction included in a processing packet to another processing target instruction included in a different processing packet, the position of the next processing target instruction to be executed is not reliably known. By contrast, claims 1 and 49 recite that the position of a next processing target instruction is known easily and reliably with the second program counter cycling through a number of different values where the number is any number except for a power of 2. Hence, the Christie reference does not disclose, teach or suggest a second program counter indicating a position of processing target instruction in the processing packet by using the same number of values as the number of processing target instructions, and cycling through the values as recited in claims 1 and 49.

For at least the reasons discussed above, Applicants submit that the invention recited in claims 1-11 and 49 is patentably distinguishable over the cited Christie reference and the prior art of record. Additionally, all dependent claims are also in condition for allowance as a result of their dependence on independent claim 1.

Applicants respectfully request that the 35 U.S.C. §§ 102(a) and 103(a) rejections be withdrawn.

Added New Claim 50

For at least the reasons discussed above, Applicants submit that new claim 50 is patentably distinguishable over the cited Christie reference and the prior art of record. Therefore, new claim 50 should also be in condition for allowance.

Conclusion

In view of the remarks made above, it is respectfully submitted that the pending claims are in condition for allowance, and such action is respectfully solicited. If any matters remain outstanding after consideration of the response that the Examiner believes might be expedited by a telephone conference with Applicants' representative, he is respectfully requested to call the undersigned attorney at the number indicated.

Authorization is hereby given to charge our Deposit Account No. 19-2814 for any charges that may be due. Furthermore, if an extension is required, then Applicants hereby request such an extension.

Respectfully submitted,

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I hereby certify that this document and fee is being deposited on July 7, 2003 with the U.S. Postal Service as first class mail under 37 C.F.R. §1.8 and is addressed to Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450.

By: Debbie Josephson

Signature

Dated: July 7, 2003